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Inventors
Akers, Jason
Clark, Chace

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US2019235785 A1 Apparatus, systems, and methods to reclaim storage associated with cached data

Abstract Embodiments are directed towards apparatuses, methods, and systems associated with a storage reclamation manager that generates a command to reclaim storage locations to assist in management of a storage capacity of a primary storage device. In embodiments, the command is a trim command to inform the storage device of storage locations including invalid data. In embodiments, the command is generated during performance of operations associated with a write-back operation where a cache coupled with the processor stores a first portion of data and the primary storage device stores a corresponding second portion of data. In embodiments, the command is generated during or after a write-back operation of a third portion of data into the cache device. In embodiments, the command assists in reclamation of storage locations in which the second portion of data is stored, to assist in management of a storage capacity of the primary storage device. Additional embodiments may be described and claimed.

Claim 1. An apparatus, comprising:
a storage reclamation manager communicatively coupled with a cache that stores a first portion of data, and a primary storage device that stores a corresponding second portion of data, to during a write-back operation of a third portion of data into the cache, generate a command to the primary storage device to assist in reclamation of storage locations in which the second portion of data is stored, to assist in management of a storage capacity of the primary storage device.

2. The apparatus of claim 1, wherein the storage reclamation manager comprises a processor coupled to the primary storage device and the cache and wherein to assist in reclamation of the storage locations comprises to indicate the storage locations as including invalid data.

3. The apparatus of claim 2, wherein the second portion of data includes a copy of the first portion of data and the third portion of data is to modify or replace the first portion of data in the cache.

4. The apparatus of claim 3, wherein upon completion of the write-back operation of the third portion of data, the second portion of data stored in the primary storage device is indicated as invalid.

5. The apparatus of claim 4, wherein the command includes a trim command to free the storage locations by informing the primary storage device of addresses of the second portion of data.

6. The apparatus of claim 5, wherein a fourth portion of data to correspond to the third portion of data is to be stored in the primary storage device at a designated time after the write-back operation.

7. The apparatus of claim 1, wherein the command includes an unmap command to be applied to the second portion of data.

8. The apparatus of claim 1, wherein a fourth portion of data is later to be stored in the primary storage device and includes a copy of the third portion of data that is stored in the cache.

In the latter scenario, the remote computer may be connected to the user's computer through any type of network, including a local area network (LAN) or a wide area network (WAN), or the connection may be made to an external computer (for example, through the Internet using an Internet Service Provider). Note that primary embodiments include software or firmware implementations; however, as noted throughout the Description, hardware implementations are contemplated as well.

FIG. 9 is a diagram of a solid-state drive (SSD) 900 that may be included in embodiments of the disclosure. For example, in embodiments, cache devices 303 and 403 and/or primary storage device 305 and 405 of respective FIG. 3 and FIG. 4 may include one or more SSDs 900. As shown, in embodiments, an SSD includes a solid-state memory device 901 coupled to a controller 903 that includes a host interface 905 to receive a command or otherwise interface with, e.g., host or platform device 350 of FIG. 1. In some embodiments, host interface 905 receives a storage reclamation command from a storage reclamation manager (e.g., storage reclamation manager 301 or 401 of respective FIG. 3 or FIG. 4) to allow controller 903 (e.g., are of controller 903) to perform or implement operations in connection with a trim command from or associated with storage reclamation manager 301 and 401.

Accordingly, solid-state memory device 901 of SSD 900 includes any suitable solid-state memory device for storing, e.g., data associated with the write-back operations of FIGS. 3-8. In some embodiments, solid-state storage device 901 includes, e.g., a NAND device, e.g., 3D TLC (triple-level per cell) or QLC (quad-level per cell) NAND device. In some embodiments, the SSD may include a RAM with, e.g., batteries as integrated power sources to retain data for a certain time after external power is lost. In various embodiments, hybrid drives or solid-state hybrid drives (SSHDs) that combine features of SSDs and hard disk drives (HDDs) in a unit may be contemplated.

In embodiments, solid-state memory device 901 of SSD 900 includes any suitable persistent memory, e.g., a write-in-place byte addressable non-volatile memory. In embodiments, SSD 900 includes any suitable memory that stores data by changing the electrical resistance of the memory cells. In embodiments, SSD 900 can also include a byte-addressable write-in-place three dimensional crosspoint memory device, or other byte addressable or multi-level NVM device, such as single or multi-level Phase Change Memory (PCM) or phase change memory with a switch (PCMS), NVM devices that use chalcogenide phase change material (for example, chalcogenide glass), resistive memory including metal oxide base, oxygen vacancy base and Conductive Bridge Random Access Memory (CB-RAM), nanowire memory, ferroelectric random access memory (FeRAM, FRAM), magneto resistive random access memory (MRAM) that incorporates memristor technology, spin transfer torque (STT)-MRAM, a spintronic magnetic junction memory based device, a magnetic tunneling junction (MTJ) based device, a DW (Domain Wall) and SOT (Spin Orbit Transfer) based device, a thyristor based memory device, or a combination of any of the above, or other memory.

FIG. 10 is a diagram of another solid-state drive (SSD) 1000 that may be included in embodiments of the disclosure. In embodiments, SSD 1000 includes both a solid-state memory device 1001 as a cache device and a solid-state memory device 1002 as a primary storage device. As shown, in embodiments, solid-state memory device 1001 and

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US2019235785 A1 Apparatus, systems, and methods to reclaim storage associated with cached data

Abstract Embodiments are directed towards apparatuses, methods, and systems associated with a storage reclamation manager that generates a command to reclaim storage locations to assist in management of a storage capacity of a primary storage device. In embodiments, the command is a trim command to inform the storage device of storage locations including invalid **data**. In embodiments, the command is generated during performance of operations associated with a write-back operation where a cache coupled with the processor stores a first portion of **data** and the primary storage device stores a corresponding second portion of **data**. In embodiments, the command is generated during or after a write-back operation of a third portion of **data** into the cache device. In embodiments, the command assists in reclamation of storage locations in which the second portion of **data** is stored, to assist in management of a storage capacity of the primary storage device. Additional embodiments may be described and claimed.

Claim 1. An apparatus, comprising:
a storage reclamation manager communicatively coupled with a cache that stores a first portion of **data**, and a primary storage device that stores a corresponding second portion of **data**, to during a write-back operation of a third portion of **data** into the cache, generate a command to the primary storage device to assist in reclamation of storage locations in which the second portion of **data** is stored, to assist in management of a storage capacity of the primary storage device.

2. The apparatus of claim 1, wherein the storage reclamation manager comprises a processor coupled to the primary storage device and the cache and wherein to assist in reclamation of the storage locations comprises to indicate the storage locations as including invalid **data**.

3. The apparatus of claim 2, wherein the second portion of **data** includes a copy of the first portion of **data** and the third portion of **data** is to modify or replace the first portion of **data** in the cache.

4. The apparatus of claim 3, wherein upon completion of the write-back operation of the third portion of **data**, the second portion of **data** stored in the primary storage device is indicated as invalid.

5. The apparatus of claim 4, wherein the command includes a trim command to free the storage locations by informing the primary storage device of addresses of the second portion of **data**.

6. The apparatus of claim 5, wherein a fourth portion of **data** to correspond to the third portion of **data** is to be stored in the primary storage device at a designated time after the write-back operation.

7. The apparatus of claim 1, wherein the command includes an unmap command to be applied to the second portion of **data**.

8. The apparatus of claim 1, wherein a fourth portion of **data** is later to be stored in the primary storage device and includes a copy of the third portion of **data** that is stored in the cache.

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accordance with various embodiments, is shown. As illustrated, non-transitory computer-readable storage medium 802 may include the executable code of a number of programming instructions 804 (or **data** to create the programming instructions). Executable code of programming instructions 804 may be configured to enable a system, **or, computing system or computer device 700**, in **4** to execution of the executable code/programming instructions, to perform various operations associated with FIGS. 3-6. In alternate embodiments, executable code/programming instructions 804 (or **data** to create the instructions) may be disposed on multiple non-transitory computer-readable storage medium 802 instead. In still other embodiments, executable code/programming instructions 804 (or **data** to create the instructions) may be encoded in transitory computer-readable medium, such as signals.

In embodiments, a processor may be packaged together with a computer-readable storage medium having some or all of executable code of programming instructions 804 (or **data** to create the instructions) configured to practice all or selected ones of the operations earlier described with references to FIGS. 3-6. For one embodiment, a processor may be packaged together with such executable code 804 (or **data** to create the code) to form a System in Package (SIP). For one embodiment, a processor may be integrated on the same die with a computer-readable storage medium having such executable code 804 (or **data** to create the code). For one embodiment, a processor may be packaged together with a computer-readable storage medium having such executable code 804 (or **data** to create the code) to form a system on chip (SoC). For at least one embodiment, the SoC may be utilized in, **e.g., computing device 700**.

In various embodiments, the programming instructions or program code (or **data** to create the program code) described herein may be stored in one or more of a compressed format, an encrypted format, a fragmented format, a packaged format, etc. Program code (or **data** to create the program code) as described herein may require one or more of installation, modification, adaptation, updating, combining, supplementing, configuring, decryption, decompression, unpacking, distribution, reassignment, etc. in order to make it directly readable and/or executable by a computing device and/or other machine. For example, the program code (or **data** to create the program code) may be stored in multiple parts, which are individually compressed, encrypted, and stored on separate computing devices, wherein the parts when decrypted, decompressed, and combined form a set of executable instructions that implement the program code (or the **data** to create the program code) such as that described herein. In another example, the program code (or **data** to create the program code) may be stored in a state in which it may be read by a computer, but require addition of a library (e.g., a dynamic link library), a software development kit (SDK), an application programming interface (API), etc. in order to execute the instructions on a particular computing device or other device. In another example, the program code (or **data** to create the program code) may need to be configured (e.g., settings stored, **data** input, network addresses recorded, etc.) before the program code (or **data** to create the program code) can be executed/used in whole or in part. Thus, the disclosed program code (or **data** to create the program code) are intended to encompass such machine-readable instructions and/or program(s) (or **data** to create such machine-readable instruction and/or programs) regardless of the particular format or state of the machine-readable instructions and/or program(s) when stored or otherwise at

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Abstract

Embodiments are directed towards apparatuses, methods, and systems associated with a storage reclamation manager that generates a command to reclaim storage locations to assist in management of a storage capacity of a primary storage device. In embodiments, the command is a trim command to inform the storage device of storage locations including invalid **data**. In embodiments, the command is generated during performance of operations associated with a write-back operation where a cache coupled with the processor stores a first portion of **data** and the primary storage device stores a corresponding second portion of **data**. In embodiments, the command is generated during or after a write-back operation of a third portion of **data** into the cache device. In embodiments, the command assists in reclamation of storage locations in which the second portion of **data** is stored, to assist in management of a storage capacity of the primary storage device. Additional embodiments may be described and claimed.

Claim

1. An apparatus, comprising:
a storage reclamation manager communicatively coupled with a cache that stores a first portion of **data**, and a primary storage device that stores a corresponding second portion of **data**, to during a write-back operation of a third portion of **data** into the cache, generate a command to the primary storage device to assist in reclamation of storage locations in which the second portion of **data** is stored, to assist in management of a storage capacity of the primary storage device.

2. The apparatus of claim 1, wherein the storage reclamation manager comprises a processor coupled to the primary storage device and the cache and wherein to assist in reclamation of the storage locations comprises to indicate the storage locations as including invalid **data**.

3. The apparatus of claim 2, wherein the second portion of **data** includes a copy of the first portion of **data** and the third portion of **data** is to modify or replace the first portion of **data** in the cache.

4. The apparatus of claim 3, wherein upon completion of the write-back operation of the third portion of **data**, the second portion of **data** stored in the primary storage device is indicated as invalid.

5. The apparatus of claim 4, wherein the command includes a trim command to free the storage locations by informing the primary storage device of addresses of the second portion of **data**.

6. The apparatus of claim 5, wherein a fourth portion of **data** to correspond to the third portion of **data** is to be stored in the primary storage device at a designated time after the write-back operation.

7. The apparatus of claim 1, wherein the command includes an unmap command to be applied to the second portion of **data**.

8. The apparatus of claim 1, wherein a fourth portion of **data** is later to be stored in the primary storage device and includes a copy of the third portion of **data** that is stored in the cache.

FIG. 9 is a diagram of a solid-state drive (SSD) 900 that may be included in embodiments of the disclosure. For example, in embodiments, cache devices 303 and 403 and/or primary storage device 305 and 405 of respective FIG. 3 and FIG. 4 may include one or more SSDs 900. As shown, in embodiments, an SSD includes a solid-state memory device 901 coupled to a controller 903 that includes a host interface 905 to receive a command or otherwise interface with, e.g., host or platform device 350 of FIG. 1. In some embodiments, host interface 905 receives a storage reclamation command from a storage reclamation manager (e.g., storage reclamation manager 301 or 401 of respective FIG. 3 or FIG. 4) to allow controller 903 (e.g., firmware of controller 903) to perform or implement operations in connection with a trim command from or associated with storage reclamation manager 301 and 401.

Accordingly, solid-state memory device 901 of SSD 900 includes any suitable solid-state memory device for storing, e.g., data associated with the write-back operations of FIGS. 3-6. In some embodiments, solid-state storage device 901 includes e.g., a NAND device, e.g. 3D TLC (triple-level per cell) or QLC (quad-level per cell) NAND device. In some embodiments, the SSD may include a RAM with, e.g., batteries as integrated power sources to retain data for a certain time after external power is lost. In various embodiments, hybrid drives or solid-state hybrid drives (SSHDs) that combine features of SSDs and hard disk drives (HDDs) in a unit may be contemplated.

In embodiments, solid state memory device 901 of SSD 900 includes any suitable persistent memory, e.g., a write-in-place byte addressable non-volatile memory. In embodiments, SSD 900 includes any suitable memory that stores data by changing the electrical resistance of the memory cells. In embodiments, SSD 900 can also include a byte-addressable write-in-place three dimensional crosspoint memory device, or other byte addressable write-in-place NVM device, such as single or multi-level Phase Change Memory (PCM) or phase change memory with a switch (PCMS), NVM devices that use chalcogenide phase change material (for example, chalcogenide glass), resistive memory including metal oxide base, oxygen vacancy base and Conductive Bridge Random Access Memory (CB-RAM), nanowire memory, ferroelectric random access memory (FeRAM, FRAM), magnetoresistive random access memory (MRAM) that incorporates memristor technology, spin transfer torque (STT)-MRAM, a spintronic magnetic junction memory based device, a magnetic tunneling junction (MTJ) based device, a DW (Domain Wall) SOT (Spin Orbit Transfer) based device, a thyristor based memory device, or a combination of any of the above, or other memory.

FIG. 10 is a diagram of another solid-state drive (SSD) 1000 that may be included in embodiments of the disclosure. In embodiments, SSD 1000 includes both a solid-state memory device 1001 as a cache device and a solid-state memory device 1002 as a primary storage device. As shown, in embodiments, solid-state memory device 1001 and solid-state memory device 1002 are coupled to a host interface 1006 to receive a command or otherwise interface with, e.g., host or platform device 350 of FIG. 1. In some embodiments, host interface 1006 receives a storage reclamation command from a storage reclamation manager (e.g., storage reclamation manager 301 or 401 of respective FIG. 3 or FIG. 4) to allow interface(s) 1006 to perform or implement operations in connection with a trim command, unmap, or other storage optimization command from or

Tools

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1. Image shows 2 out of 3 highlighted parts.
2. An blue (P) on the scrollbar indicates where these passages are found.
 - a. Click on the blue (P) to quickly navigate to that passage.

Note

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