

Family legal status indicator *

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The screenshot displays the IPSCREENER interface, which is used for patent search and analysis. The interface is divided into several sections:

- Left Sidebar:** Contains navigation links such as "Search new idea", "My ideas", "Admin", "My profile", "Support", "Export", "My Evaluation", "Quick view", "Highlight", and "Log out".
- Top Bar:** Shows the current search criteria, including "Idea", "Version 1 / 1", and "Sep 29, 2020 05:49".
- Main Content Area:** Displays search results for patents. The first result is for patent #1 US2019235785 A1, titled "Apparatus, systems, and methods to reclaim storage associated with cached data". The second result is for patent #2 US10430108 B2, titled "Concurrent copying of first and second subsets of pages from media such as s1c and to media such as q1c or m1c and for completion of copying of data".
- Right Sidebar:** Contains various charts and graphs, including a world map, a bar chart showing "2018 Value: 111", and a line graph showing "2010 Value: 111".

Key features of the interface include:

- Search Filters:** Users can filter results by "Title of the idea", "Text describing the idea", "Publication date", "Priority date", "Applicant", "Inventor", "IPC/CPC Class", and "Screening Batch List".
- Patent Details:** Each patent entry includes a title, abstract, passage, and claim. The first patent's abstract describes a storage reclamation manager that generates a command to reclaim storage locations to assist in management of a storage capacity of a primary storage device.
- Family Legal Status Indicator:** A red box highlights the "FAMILY LEGAL STATUS INDICATOR" section for each patent. This section indicates the status of the patent family, such as "AND FIRST PRIORITY" and "FAMILY LEGAL STATUS INDICATOR".
- Visual Indicators:** A red circle with the number "1" is placed over the "FAMILY LEGAL STATUS INDICATOR" section of the second patent entry, indicating that the indicator is displayed in full-size view as colored text.

1. Display if a patent is Alive (green) or Dead (red).
2. Indicator are found on all patents grey info box under Family legal status indicator.
 - a. Also displayed in fullsize view as coloured text, under Family legal status indicator. See image below.

IPSCREENER

AutoPatent Technology

Biblio data

Status indicator

Patent application

First published

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by

INTEL CORP.; INTEL CORPORATION;

and first priority

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Inventors

Akers, Jason

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IPC Classes

G06F3/06

Family Members

US2019235785 A1

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Version 2.7.0

US2019235785 A1 Apparatus, systems, and methods to reclaim storage associated with cached data

Abstract Embodiments are directed towards apparatuses, methods, and systems associated with a storage reclamation manager that generates a command to reclaim storage locations to assist in management of a storage capacity of a primary storage device. In embodiments, the command is a trim command to inform the storage device of storage locations including invalid **data**. In embodiments, the command is generated during performance of operations associated with a write-back operation where a cache coupled with the processor stores a first portion of **data** and the primary storage device stores a corresponding second portion of **data**. In embodiments, the command is generated during or after a write-back operation of a third portion of **data** into the cache device. In embodiments, the command assists in reclamation of storage locations in which the second portion of **data** is stored, to assist in management of a storage capacity of the primary storage device. Additional embodiments may be described and claimed.

Claim 1. An apparatus, comprising:

a storage reclamation manager communicatively coupled with a cache that stores a first portion of **data**, and a primary storage device that stores a corresponding second portion of **data**, to during a write-back operation of a third portion of **data** into the cache, generate a command to the primary storage device to assist in reclamation of storage locations in which the second portion of **data** is stored, to assist in management of a storage capacity of the primary storage device.

2. The apparatus of claim 1, wherein the storage reclamation manager comprises a processor coupled to the primary storage device and the cache and wherein to assist in reclamation of the storage locations comprises to indicate the storage locations as including invalid **data**.

3. The apparatus of claim 2, wherein the second portion of **data** includes a copy of the first portion of **data** and the third portion of **data** is to modify or replace the first portion of **data** in the cache.

4. The apparatus of claim 3, wherein upon completion of the write-back operation of the third portion of **data**, the second portion of **data** stored in the primary storage device is indicated as invalid.

5. The apparatus of claim 4, wherein the command includes a trim command to free the storage locations by informing the primary storage device of addresses of the second portion of **data**.

6. The apparatus of claim 5, wherein a fourth portion of **data** is to correspond to the third portion of **data** is to be stored in the primary storage device at a designated time after the write-back operation.

7. The apparatus of claim 1, wherein the command includes an unmap command to be applied to the second portion of **data**.

8. The apparatus of claim 1, wherein a fourth portion of **data** is later to be stored in the primary storage device and includes a copy of the third portion of **data** that is stored in the cache.

FIG. 9 is a diagram of a **solid-state drive (SSD) 900** that may be included in embodiments of the disclosure. For example, in embodiments, cache devices 303 and 403 and/or primary storage device 305 and 405 of respective FIG. 3 and FIG. 4 may include one or more **SSDs 900**. As shown, in embodiments, an SSD includes a **solid-state memory device 901** coupled to a controller 903 that includes a host interface 905 to receive a command or otherwise interface with, e.g., host or platform device 350 of FIG. 1. In some embodiments, host interface 905 receives a storage reclamation command from a storage reclamation manager (e.g., storage reclamation manager 301 or 401 of respective FIG. 3 or FIG. 4) to allow controller 903 (e.g., firmware of controller 903) to perform or implement operations in connection with a trim command from or associated with storage reclamation manager 301 and 401.

Accordingly, **solid-state memory device 901 of SSD 900 includes any suitable solid-state memory device for storing, e.g., data associated with the write-back operations of FIGS. 3-6. In some embodiments, solid-state storage device 901 includes e.g., a NAND device, e.g., 3D TLC (triple-level per cell) or QLC (quad-level per cell) NAND device. In some embodiments, the SSD may include a RAN with, e.g., batteries as integrated power sources to retain data for a certain time after external power is lost. In various embodiments, hybrid drives or solid-state hybrid drives (SSHDs) that combine features of SSDs and hard disk drives (HDDs) in a unit may be contemplated. In embodiments, solid state memory device 901 of SSD 900 includes any suitable persistent memory, e.g., a write-in-place byte addressable non-volatile memory. In embodiments, SSD 900 includes any suitable memory that stores data by changing the electrical resistance of the memory cells. In embodiments, SSD 900g also include a byte-addressable write-in-place three dimensional crosspoint memory device, or other byte addressable write-in-place NVM device, such as single or multi-level Phase Change Memory (PCM) or phase change memory with a switch (PCMS), NVM devices that use chalcogenide phase change material (for example, chalcogenide glass), resistive memory including metal oxide base, oxygen vacancy base and Conductive Bridge Random Access Memory (CB-RAM), nanowire memory, ferroelectric random access memory (FeRAM, FRAM), magneto resistive random access memory (MRAM) that incorporates memristor technology, spin transfer torque (STT)-MRAM, a spintronic magnetic junction memory based device, a magnetic tunneling junction (MTJ) based device, a DW (Domain Wall) and SOT (Spin Orbit Transfer) based device, a thyristor based memory device, or a combination of any of the above, or other memory.**

FIG. 10 is a diagram of another **solid-state drive (SSD) 1000** that may be included in embodiments of the disclosure. In embodiments, SSD 1000 includes both a **solid-state memory device 1001** as a cache device and a **solid-state memory device 1002** as a primary storage device. As shown, in embodiments, **solid-state memory device 1001 and**

Tools

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Note

*This is a premium feature